**Terms and Definition**

* “Ground plane” has voltage potential ‘0V’, it’s the plane form of the ground line. Other than used as return path for electrical signal (same as ground line) in single ended transmission, it is also good for absorbing circuit noise.
* “Latching in data” refers to the device reading the data from the data line/bus.
* UART Baud rate (bits per second). Rate in which UART transmitter transmit information (START, STOP , DATA, PARITY).
* Data rate = Data transfer rate = Effective Data transfer rate = rate in which ‘data’ is transferred.
* Memory units
  + 1KByte = 2^10 Bytes
  + 1MByte = 2^20Bytes
  + 1GByte = 2^30 Bytes
  + 1Kbps = 1000bps (bits per sec)
  + 1Mbps = 1000000bps
  + 1KB/s = (2^10)bits/sec = 1024bits/sec
* System Memory = Main Memory = Physical Memory.
* Cache block = cache line = one ‘row’ of cache in the cache diagram.
* Offset (Cache) = the relative position of the target byte from the start of the cache block.
* Offset (VM) = the relative position of the target byte from the start of the virtual page or physical frame.
* ‘PAGE’ field in VM refers to the Page Number of the Virtual Page which contains the target byte.
* ‘FRAME’ field in VM refers to the Frame Number of the Physical Frame which contains the target byte.
* Virtual Memory address = the address that program code use. Virtual memory address is a logical entity, it is “not real”. OS will translate the virtual address to a physical address that is use to locate the required code/data in the physical memory (this is the ‘real’ memory where code/data are stored). Check the forum for detail description of the whole process, under the thread “Virtual memory” dated 3/23/22 2:21pm).
* Physical Memory address = address where code/data is stored in the Physical/Main/System memory during runtime.
* Cache stores frequently used code/data.
* TLB stores frequently used VirtualPage to PhysicalFrame translation information.
* TLB is a subset of the PAGE TABLE (resided in Main Memory). Page Table contains entries for all virtual pages (valid and invalid).
* “Memory types” refers to SRAM, DRAM, NOR Flash, NAND Flash, HDD etc.
* “System and Storage Memory” are functional partition of the computer memory system. System memory stores runtime code/data and processor execute code directly from it. Storage memory ‘stores’ all code/data and processor doesn’t execute code directly from it.
* “Internal memory” is a group of memories that are ‘internal’ to the processor, it is part of the processor, together with the CPU, cache, TLB etc. This versus external memory which is a separate chip from the processor.
* ‘Peripheral’ is a term used to describe a module within the processor. E.g. UART peripheral is a module that take care of the UART interface.
* For a 4-stage pipeline: F, D, E and S.
  + Fetch: Instruction (machine code) is fetched into the pipeline
  + Decode: The machine code is decoded to know which instruction it correspond to.
  + Execute: The instruction is executed, e.g. ADD, SUB operations.
  + Store: The result of the instruction execution is stored to the corresponding destination register or memory.
* You can assume the status flag is updated at the E-stage of a pipeline unless otherwise stated.
* “Delay slots” are the slots after a Branch instruction that may be flushed if the branch is TRUE.
  + There are two delay slots if the branch decision and target is resolved at the E-Stage.
  + If the branch decision and target is resolve at the D-Stage, there is only one delay slot.
* Instruction located in the delay slot is know as the delay slot instruction.
* For pipeline related questions, all the ‘ARM’ instructions presented will affect the status flag, i.e. ADD = ADDS, MOV = MOVS etc.
* Explanation of the bullet items in pipeline question
  + Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). Assume that
    - Branch target address is calculated at the execute stage
      * Branch decision and target address is resolved at the E-Stage.
    - Instruction length for every instruction is one word long
      * To simplify pipeline analysis, implies that each instruction only occupies one row of the pipeline diagram.
    - Each pipeline stage takes 1 cycle to complete
      * In pipeline processor, one pipeline stage takes 1 CPU cycle, so the first instruction needs 4 cycles to travel through the whole pipeline.
    - No resource conflicts
      * Do not give “Resource Conflict” as your answer, it won’t be accepted.
    - Delayed branching is disabled.
      * If delayed branching is disabled, that means instructions in the delay slot will be discarded if the branch is TRUE.
    - This processor is not an ARM processor. All instructions will update the relevant status flags.
      * Only consider the function of the ‘ARM’ assembly instructions you see in the question. All instructions in the question are one word long and all will affect the status bits (where applicable).
* “Channel Bandwidth” refers to the frequency range used for transmission. Note that ‘2.4 GHz’ is not a single point frequency, it encompassed a range of frequency from around 2.4Ghz to 2.48 Ghz. This range is further divided in ‘channels’ of around 22Mhz each in bandwidth for Wifi Standard, e.g. Channel 6 is a RF channel with 22-Mhz bandwidth channel, centered at 2.437Ghz.
* Typically, higher bandwidth means
  + Higher possible data transfer rate if there are no interference.
  + Higher chance of being interfered by other RF transmitters.
  + You can visualise bandwidth as the diameter of a water pipe, larger diameter, more water flow but higher chance to encounter interference.
* “Royalty” is amount of fees paid to use a particular service or product. In this case, the RF frequency band.
* “Attenuation” refers to the drop in RF signal amplitude as RF wave travels across the medium e.g. air.
* “Interference” occurs when two RF waves meet and cause some constructive or destructive interference to each other. It occurs even if the two waves are carrying signals from different standards, e.g. Wifi and Bluetooth.